Surface Plasmonic XOR Logic Gate Based on Two Mode Interference

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Abstract—*In this paper, we have proposed a compact all-optical XOR logic gate using two-mode interference in a surface plasmonic waveguide structure consisting of silicon core, silver upper and lower cladding, and GaAsInP left and right cladding. The propagation of excited SPP modes in the TMI region is controlled by refractive index modulation of GaAsInP cladding with incident optical pulse energy. The optical pulse dependent coupling behavior of the structure is studied and the XOR logic gate behavior has been shown. The proposed gate is found to be compact in size.*

1. INTRODUCTION

High performance all-optical logic gates have become key components in optical computing and networking systems to perform a majority of optical signal processing functions [1]. All-optical XOR logic gate is a main building block of optical processor devices [2]. Various technologies have been reported to realize all-optical XOR logic operation, but most of them suffer from limitations such as large size [3], random polarization changes [4] and instability [5-8]. Recently, surface plasmon polariton (SPP) based waveguide devices [6-10] have attracted enormous attention due to their compactness over photonic devices. In this paper, we have proposed a compact structure for all-optical XOR logic operation based on a surface plasmonic two mode interference (SPTMI) waveguide coupler by using nonlinear refractive index modulation of cladding area.

2. DESIGN AND CONCEPT

Fig-1 shows the basic structure of the proposed XOR logic gate device based on a surface plasmonic two-mode interference (SPTMI) waveguide made up of silicon core and GaAsInP side claddings sandwiched between two layers of silver, and having width w_T, thickness t and coupling length $2L$ and access waveguides of width w and thickness t. An optical pulse absorbing layer of PbS nanoparticle doped silica glass [11] is used in the GaAsInP region halfway along the length of the coupler (as shown in the figure)) to prevent optical pulse incident in the first GaAsInP cladding region from entering into the second GaAsInP cladding region. The refractive index $n_2(E)$ of GaAsInP shows nonlinear change depending on applied optical pulse of energy E and is written as [12]

$$n_2(E) = n_2(0) + \frac{n_{nl}E}{1.605 A_C T_P} \tag{1}$$

where, $n_2(0)$ is the refractive index of GaAsInP when no optical pulse is applied. The n_{nl} =-2×10^{-3}μm^{2}W^{-1} is the nonlinear index coefficient of GaAsInP, T_P is the full width at half maximum power of pulse, and A_C is effective cladding area of GaAsInP.

The power P_1 and P_2 are incident at the input access waveguides of the SPTMI coupler. Optical pulse power P_{C1} corresponding to optical pulse of energy E_1 and pulse width T_P is applied at the first GaAsInP cladding region, whereas, optical pulse power P_{C2} corresponding to optical pulse of energy E_2 and pulse width T_P is applied at the second GaAsInP cladding region (as shown in Fig-1). The output power at access waveguide-3 and waveguide-4 are obtained as P_3 and P_4 respectively.

(a)

(b)
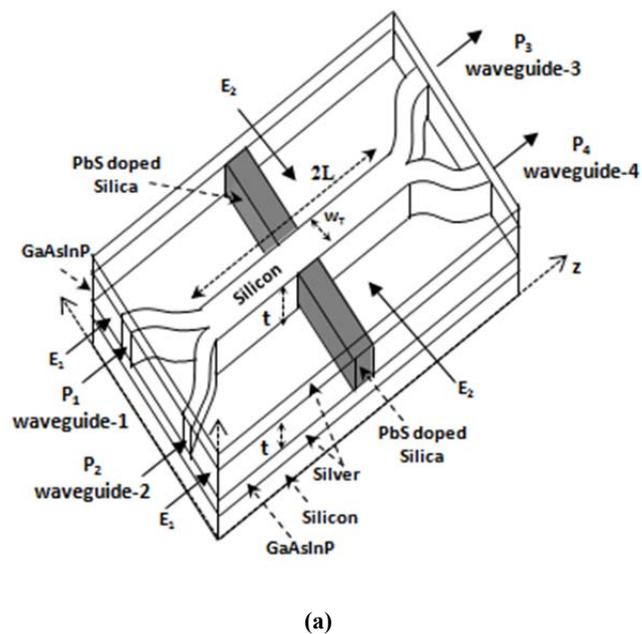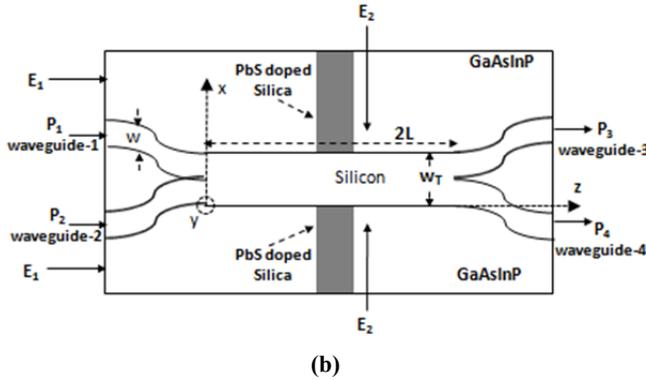
Fig. 1: 3D schematic view of XOR logic device based on surface plasmonic two-mode waveguide coupler with core width w_T, thickness t and coupling length $2L$ (a) Three dimensional view and (b) Top view of the dielectric layer

For XOR logic gate operation, the optical pulses of energy E_1 (optical pulse power P_{C1}) and E_2 (optical pulse power P_{C2}) are taken as the input signals and the power P_2 launched into the input access waveguide-2 is used as control signal. The output power P_3 at access waveguide-3 is taken as the output of the device, whereas input access waveguide-1 and output access waveguide-4 are not used.

When the input field is incident at input access waveguide-1, SPP fundamental and first order modes are excited which propagate through the two-mode coupling region at different phase velocities. The phase difference between the two coupled SPP modes at $z=L$ at the end of the coupling region depends on the length of coupling region and can be written as [9,10]

$$\Delta\phi(0) = \left[\beta_0\left(n_2(0)\right) - \beta_1\left(n_2(0)\right)\right]L \qquad (2)$$

where, $\beta_0(n_2(0))$ and $\beta_1(n_2(0))$ are the propagation constants of the fundamental and first order SPP modes respectively when no optical pulse is applied. When optical pulse of energy E and width T_P is applied at the the GaAsInP cladding, refractive index modulation of GaAsInP cladding occurs which introduces an additional phase change between the two coupled SPP modes. The phase difference between the two excited modes after application of optical pulse of energy E is written as [9,10]

$$\Delta\phi(E) = \left[\beta_0\left(n_2(E)\right) - \beta_1\left(n_2(E)\right)\right]L$$
$$= \Delta\phi(0) + \frac{2\pi L}{\lambda}\left[\Delta n_1^{eff}(E) - \Delta n_0^{eff}(E)\right] \qquad (3)$$

where, $\Delta n_0^{eff}(E)$ and $\Delta n_1^{eff}(E)$ are the effective refractive index changes for the fundamental and first order modes respectively and are given as

$$\Delta n_i^{eff}(E) = n_i^{eff}(0) - n_i^{eff}(E) \qquad (4)$$

where $i=0$ and 1 denote the fundamental and first order mode respectively. The $n_i^{eff}(0)$ and $n_i^{eff}(E)$ are the effective refractive

indices of the ith mode (i=0,1) before and after application of modulating optical pulse respectively. The length of coupling region required to get an additional π phase shift due to application of optical pulse of energy E (i.e., $\Delta\phi(E)=\pi$) can be written as [9,10]

$$L = \frac{\lambda}{2\left\{\Delta n_1^{eff}(E) - \Delta n_0^{eff}(E)\right\}} \qquad (5)$$

The structure is numerically analyzed using effective index method [9,10] and the behaviour of the various eigen modes is studied. From effective index analysis of the basic device, it is seen that the first order mode appears at w_T=0.45μm, whereas the second order mode appears at w_T=0.88μm. Thus, for two-mode propagation, the waveguide core width is chosen as w_T=0.48μm. Moreover, previous analysis of the device using effective index methods [9,10] have shown that as the core thickness increases, propagation length also increases. Thus, to ensure better output intensity, core thickness is taken as t=5.0μm. For w_T=0.48μm, t=5.0μm and a coupling length L=92.35μm, the optical pulse energy required to get an additional phase shift of π (and hence, for the switching of logic states) is estimated as E=16.04pJ. Thus the optical pulse energy for logic 'high' state (or logic '1') is taken as E=16.04pJ, whereas the optical pulse energy for logic 'low' state (or logic '0') is E=0. The device shows cross state coupling corresponding to the coupling length L=92.35μm.

Fig. 2 shows the variation of normalized output power (P_3/P_2) versus optical pulse energy E_1 of optical pulse power P_{C1} for n_1= 3.5, $n_2(0)$=3.17, n_m=0.394+8.2j, λ=1.33μm, $2w$=0.48μm, t=5.0μm, T_P=1ps, and A_C=2.0μm², and considering the optical pulse energy E_2 of optical pulse power P_{C2} as E_2=0 (logic '0') and E_2=16.04pJ (logic '1'). It is seen from the figure that for E_2=0, the output P_3/P_2 due to applied optical pulse energy
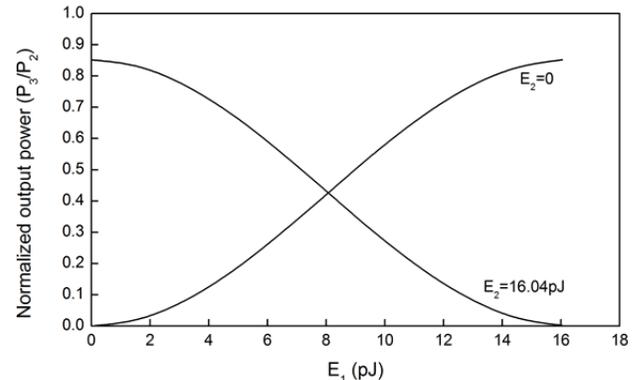
Fig. 2: Normalized output power (P_3/P_2) versus optical pulse energy E_1 of optical pulse P_{C1} for the SPTMI waveguide coupler based XOR logic gate device with n_1= 3.5, $n_2(0)$=3.17, n_m=0.394+8.2j, λ=1.33μm , w_T=0.48μm, t=5.0μm and L=92.35μm and effective cladding area A_C=2.0 μm² considering E_2=0 (logic '0') and E_2=16.04pJ (logic '1').

E_1=0 is approximately zero, and reaches a maximum with applied optical pulse energy E_1=16.04pJ, whereas for

E_2=16.04pJ, the output P_3/P_2 with E_1=0 is maximum and becomes very small when optical pulse energy E_1 increases to 16.04pJ. Thus, it is evident from the figure that the output is 'high' when only one of the inputs is high (combinations (0,1) and (1,0)). When both the inputs are 'low' (combination (0,0)) or 'high' (combination (1,1)) at the same time, the output is low. So, the output power P_3 in the proposed device shows XOR logic gate operation. The operation of the device can explained as follows:

When E_1=E_2=0 (P_{C1}=P_{C2}=0), no optical pulse is applied to the cladding of the device, and hence there is no resultant cladding index modulation. As the device shows bar state coupling, no power is obtained at output access waveguide-3 (P_3=0) due to absence of power at input access waveguide-1. When E_1=E_2=16.04pJ (P_{C1}=P_{C2}=1), cladding index modulation occurs in the device due to optical pulse applied to both the first cladding region (0<L<92.35μm) and second cladding region (L>92.35μm). Thus both the regions show bar state coupling leading to bar state coupling of the complete device. No power is obtained at output access waveguide-3 (P_3=0) due to absence of power at input access waveguide-1.

When E_1=0 (P_{C1}=0) and E_2=16.04pJ (P_{C2}=1), no optical pulse is applied to the first cladding region and hence the device shows cross state coupling for 0<L<92.35μm, whereas the device shows bar state coupling for L>92.35μm due to application of optical pulse power to the second cladding region. Thus, the output is obtained at cross state and P_3 is 'high' due to transfer of power from input access waveguide-2 (P_3=1). When E_1=16.04pJ (P_{C1}=1) and E_2=0 (P_{C2}=0), the device shows bar state coupling for 0<L<92.35μm due to application of optical pulse power to the first cladding region, whereas the device shows cross state coupling for, L>92.35μm as no optical pulse is applied to the first cladding region. This leads to cross state coupling of the complete device and the output P_3 is obtained as 'high' due to transfer of power from input access waveguide-2 (P_3=1).

Table 1: Truth table for the proposed XOR logic gate

Control signal		Input signal		output
P_1	P_2	P_{C1}	P_{C2}	P_3
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0

Thus, the output of the device shows XOR logic gate behaviour. The various combinations of input-output logic states are shown in Table-1.

3. CONCLUSION

In this paper, we have proposed an XOR logic gate device using a surface plasmonic two-mode interference coupler waveguide consisting of silicon core, silver upper and lower cladding and GaAsInP as the left and right claddings, to operate at the wavelength of 1.33μm. Switching of logic high and low states is achieved by applying optical pulse which causes refractive index modulation of GaAsInP cladding and thus introduces an additional phase change between the coupled SPP modes. The total length of the proposed device is found to be ~5.11 times compact than that of MMINDC based all-optical XOR/XNOR logic gate devices [3]. The designed XOR logic device is free from any instability caused by any unwanted variation of input phase difference as the output power does not depend on the phase difference of input signals,. The designed XOR logic gate is found to have a considerable value of fabrication tolerance.

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